

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE
SHEET INDEX	1	2
SUPPORTING INFORMATION		
NOTES		
USED-ON TABLE		
CURRENT DRAIN		
RECORD OF CHANGES		
CIRCUIT SCHEMATIC	2	2
COMPONENT LIST	3	2
CIRCUIT DESCRIPTION	4	2

SYMBOL
BUFFER A
ELEMENT IDENT
A

TERM. MOD	FUNCT	TERM.	LOC.	TERM. MOD	FUNCT	TERM.	LOC.
ACK10	I	308	247	1NF120	#	213	347
BLK CORR	I	005	348	1NF130	#	306	349
BPFL0	I	207	349	1NF140	#	206	349
SR0	I	004	248	1NF150	#	300	342
BUSV0	I	102	243	1N190	#	017	348
CL4	I	305	247	LC1P1	#	203	345
GPR0	I	019	246	1W400	#	215	347
1AKT0	I	008	349	1W5T41	#	204	340
1WFO00	I	013	241	RD0	#	205	240
1WFO10	I	113	241	RT, AC RAD	#	003	245
1WFO20	I	014	241	RT, ADRCO	#	100	246
1WFO30	I	114	241	RT, ADRCO	#	002	246
1WFO40	I	012	241	ST, CLAO	#	108	241
1WFO50	I	112	240	ST, UPF0	#	212	346
1WFO60	I	217	347	SAB1	#	009	344
1WFO100	I	216	347	SYNCO	#	103	242
1WFO110	I	011	346	TG, SEQ1	#	010	345
1WFO120	I	313	346	UNLBRAD	#	209	346
1WFO130	I	007	340	W4T0	#	015	244
1WFO140	I	106	340	+5	P	000, 119	242
1WFO150	I	006	340	GR0	G	200, 319	244
1WFO160	I	107	241				
1WFO170	I	318	246				
PE1	I	001	240				
RC0	I	118	242				
RD0	I	115	243				
SD0	I	018	242				
SC0	I	116	243				
SP1ILLO	I	104	342				
C, SH1	#	105	344				
CLC01	#	309	341				
CLC11	#	008	341				
CSTC1	#	111	344				
OV, FILL1	#	110	340				
ENDT0	#	109	345				
END	#	304	240				
GPO	#	117	246				
70ND0	#	016	248				
1WFO60	#	101	343				
1WFO70	#	102	343				
1WFO80	#	201	342				
1WFO90	#	315	348				
1WFO100	#	314	348				
1WFO110	#	214	348				

RECORD OF CHANGES

DATE	PREV	STO	HYD	SEE
ISS	FURN		DISC	NOTE

SYSTEMS	DESIGN
LISTED ON	CONTENTS
COMMON	IN
SYSTEMS	

CURRENT DRAIN: 380mA

NOTES:

1. GROUP RETURN

2. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS
CAPACITANCE VALUES ARE IN MICROFARADS
VALUES PRECEDED BY THE SYMBOL "(PL 5)"
OR "(MINUS)" ARE IN VOLTS

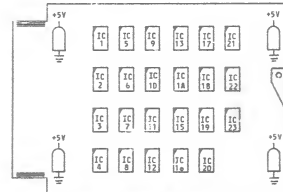
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC	BAT.	GRD
CODE	TERM.	TERM.
AT42	16	7, 8
AT4P	16	8
AT4B	16	7, 8
AT4C	16	8
AT4D	16	8
AT4E	16	7, 8
AT4F	16	8
AT4G	16	7, 8
AT4H	16	7, 8
AT4I	16	8
AT4J	16	8
AT4K	16	8
AT4L	16	8
AT4M	16	8
AT4N	16	8
AT4O	16	8
AT4P	16	8
AT4Q	16	8
AT4R	16	8
AT4S	16	8
AT4T	16	8
AT4U	16	8
AT4V	16	8
AT4W	16	8
AT4X	16	8
AT4Y	16	8
AT4Z	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000, 119
GRD	200, 319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.

6. INTEGRATED CIRCUIT LOCATION GUIDE:
(COMPONENT SIDE SHOWN)

UNMARKED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK10
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (EARLY HIGHER SERIES IS ACCEPTABLE).	
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

- WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
- THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
- THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET
- SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
- THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING IS A WHOLE.

NOTICE—NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

JK10 CIRCUIT PACK

BUFFER A
CIRCUIT

1WFO

AT420

STANDARD

2

CPS-JK10

4 SHEETS

BELL TELEPHONE LABORATORIES

65

LETTER A



BUFFER A



PART OF CPS JK10 BUFFER A

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELER	IC1 41CA	IC2 41CA	IC3 41CA	IC4 41CA	IC5 41BP	IC6 41BP	IC7 41BP	IC8 41CA	IC9 41U	IC10 41CF	IC11 41BP	IC12 41BP		
DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	
A	GRD	266	ST.TFPO	368	ST.ACTO	369	ST.RYD	362	GPRI	286	ITPI	367	STATUS1B	275
B	IDDMO	268	ST.ULPO	368	RYD	260	ST.FILO	362	RC1	262	LRABO	367	DEFL1	189
C	WITD	264	ST.STFO	367	END	260	ST.PTFO	363	SS11	263	STUFF	364	STUFF	364
D	INTPO	268	ST.LDO	368	ST.BFLO	369	ST.BRO	363	E.SST1	265	STUFF2	366	LOITR1	365
E									RDI	263	UNLBARO	366	CLK1	207
F									S01	262	UNLBARO	364	ACCT1	207
G									GP.RSD	264	LRABO1	367	STATUS1A	275

LOC CODE ELER	IC13 41U		IC14 41U		IC15 41U		IC16 41CD		IC17 41CE		IC18 41U		IC19 41RE		IC20 41EN		IC21 41EG		IC22 41BR		IC23 4132	
	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	E.RD	263	C.STCD	364	CLD01	361	D.CMD0	380	D.36CD1	261	SW1C	272	ULCL1A7B	294	RG11	270	IMP4C	201	C.57C1	364	CL.880	314
B	BF.WTD	204	E.STUFO	363	CLD00	361			OV.FLL1	360	ULCL1A7B	294	WST4D	300					C.57C1	364	CL.880	314
C	E.SSD	203	ERT	270	CLC10	361			16.SCQ1	365				300						300		
D	E.RCD	262	E.UNLRO	363	CLC11	361			L.STA1	304			RLC.WTD	278	IMP51	280			CL.881	363		
E																						
F																						
G																						

CAPACITOR

DESIG	CODE
(4) C1-C4	601A, 5
(23) C5-C27	KS-19774 L1A, L1

RESISTOR

DESIG	CODE
(2) R1, R2	KS-20616 L1A, L1A, 400
R3	KS-20616 L1A, 1M0
R4	KS-20616 L1A, L1, 400

CIRCUIT DESCRIPTION

CIRCUIT PACK JK10 HANDLES THE BUFFER ADDRESS AND COMMAND DECODING AND HANDSHAKING ON THE COMMON PARALLEL BUS. BUFFER ADDRESS (0015) APPEARING ON BUS LEADS INFOOD-INFO5 IS DECODED BY D.36CD1 CAUSING THE ADDRESS F/F TO RESPOND TO BE CLEARED ON THE LEADING EDGE OF RCD. SELECTING THE BUFFER AND UNLBARO COMMAND INPUTS S00, S01 AND S02 AS WELL AS THE END OUTPUT. THE BUFFER IS DESELECTED (ADDRESS IS SET) EITHER BY INTD OR BY AN AC ACCOMPANYING A NONBUFFER DEVICE CODE. AN ADDRESSED CIRCUIT RETURNS SYNC IN RESPONSE TO RCD, S00, R00, OR S02 AND NEGATES SYNC FOLLOWING THE REMOVAL OF THE COMMAND SIGNAL. END IS ASSERTED BY RCD AND IS HELD TRUE BY A PARITY ERROR INDICATION (PE1 TRUE).

THE RECEPTION OF AN S02 LITES STATUS INFORMATION ONTO THE BUS AND ASSERTS WAITO AND PARITY GENERATE REQUEST GPO IN ADDITION TO SYNC. THE NEXT FALLING EDGE OF CLK SETS ULYCL1A AND THE FOLLOWING RISING EDGE SETS ULYCL1B, CUTTING OFF GPO. THE PARITY GENERATION CIRCUITS IN THE BUS TERMINATOR RESPOND BY ASSERTING GPO WHICH REMOVES STATUS INFORMATION FROM THE BUS AND INHIBITS THE BUFFER WAITO. THE DELAY CHAIN IS CLEARED WHEN S02 IS REMOVED.

R00 CLOCKS INFORMATION ON THE PARALLEL BUS INTO THE INTERMEDIATE TRANSFER REGISTER, ITR, ON J212 VIA LEAD LOITR1. S00 GATES THE ITR ONTO THE BUS VIA LEAD ENDO.

WAITO IS ASSERTED WHEN BUS01 IS ACTIVE AND THE BUFFER IS SELECTED BUT MAY BE BLOCKED AT GATE BLK.WTD BY COMMAND DECODER (D.CMD) OUTPUT 7. INTDPO IS ASSERTED WHEN BUS IS ACTIVE AND THE STATE REGISTER STP.BY BIT IS NOT SET. AN INTERRUPT CONDITION ENABLES BUFFER INTERRUPT IDENTIFICATION GATE IDEND IN RESPONSE TO AN RCD COMMAND.

D.CMD DECODES THE INFORMATION ON INFO30-INFO50 WHEN RCD IS ON TO ACTIVATE 1 OUT OF 8 DECODER OUTPUTS. OUTPUT 7 PREVIOUSLY MENT-ONED IS USED IN CONNECTION WITH A MOP COMMAND.

OUTPUT 5 CLOCKS THE BIT PATTERN ON LEAD INFO00-INFO10 INTO THE 4-BIT STATE REGISTER STATE1. THE STATE REGISTER CONTROLS THE STATES OF LEADS STUFFO, UNLBARO, LEADPO, INT.BY1 WHICH INDICATE THE TYPE OF OPERATION TO BE PERFORMED ON THE OFF-LINE INTER. OUTPUT 4 ASSERTS SW1, TOGGING THE ACT F/F ON J211 AND EFFECTING A BUFFER SWITCH. OUTPUT 3 CLOCKS THE CL.WTD F/F WHICH ASSERTS C.W1, CLEARING THE NR FLAC ON J211. CL.WTD F/F MAY BE HELD SET BY AN ACTIVE LEVEL ON J211.CW1. OUTPUT 2 ASSERTS EITHER CLC10 OR CLC11 TO CLE- THE BUFFER COUNTER INDICATED BY THE STATE OF 1A.CD1. OUTPUT 1 ASSERTS DV.FLL1 RESULTING IN A CC-INITIATED ON-LINE BUFFER FILL OPERATION. OUTPUT 0 PERFORMS BUFFER INITIALIZATION (AS DOES LEAD INTD) BY RESETTING STATE1. CLEARING BOTH ON-LINE AND OFF-LINE BUFFER COUNTERS VIA CLC10 AND CLC11, AND ASSERTING WAITO1. OUTPUT 6 OF D.CMD IS NOT USED.

CSTC1 CLEARS THE STUFF SEQUENCE COUNTER ON J211 WHILE THE LEAD BIT IN THE STATE REGISTER IS BEING SET. TO.S001 STARTS OFF-LINE SEQUENCING ON J211 IF EITHER TSL STATE REGISTER STUFF OR UNLBARO BIT IS BEING SET OR IF R00 ON S00 IS ACTIVE.

D.CMD TRUTH TABLE
(SS000 = E.RCD ACTIVE)

INFO50	INFO40	INFO30	ASSERED OUTPUT
0	0	0	7
0	0	1	3
0	1	0	5
0	1	1	1
1	0	0	6
1	0	1	2
1	1	0	4
1	1	1	0

JK10 CIRCUIT PACK

BELL TELEPHONE LABORATORIES

CPS-JK10
SHEET 4

65

201